REMARKS/ARGUMENTS

The Examiner found that claims 9, 16, and 26 would be allowed if rewritten in independent form. Applicants submit that these claims are patentable over the cited art in their current form because they depend from base claims 1, 11, and 18, which are patentable over the cited art for the reasons discussed below.

1. Claims 1-3, 5, 6, 10, 18-20, 22, 23, 27, and 28 are Patentable Over the Cited Art

The Examiner rejected claims 1-3, 5, 6, 10, 18-20, 22, 23, 27, and 28 as anticipated (35 U.S.C. §102(b)) by Adkisson (U.S. Patent No. 5,590,304). Applicants traverse for the following reasons.

Claims 1 and 18 concern managing requests to an Input/Output (I/O) device, and require: queuing I/O requests directed to the I/O device; determining whether a number of queued I/O requests exceeds a threshold; calculating a coalesce limit in response to determining that the number of queued I/O requests exceeds the threshold; coalescing a number of queued I/O requests not exceeding the calculated coalesce limit into a coalesced I/O request; and transmitting the coalesced I/O request.

Applicants amended claims 1, 11, and 18 to clarify that the coalesce limit is calculated in response to determining that the number of queued I/O requests exceeds the threshold. This amendment was discussed with the Examiner and the Examiner said he would review the rejection in view of the amendment and arguments.

The Examiner cited col. 5, lines 35-45 of Adkisson as disclosing the claim requirement of determining whether a number of queued I/O requests exceeds a threshold. (Second Office Action, p. 2) Applicants traverse.

The cited col. 5 mentions that memory requests are received at an I/O queue . The requests to the queue 102 are outputted at a selected clock rate that is a multiple of the clock rate at which the memory units 103 inputs memory requests. When the memory clock rate exceeds the I/O output clock rate, queue 200 queues a number of memory requests, after which the queued requests are output to the memory unit 103 as a burst. Although the cited col. 5 discusses a queue 200 bursting I/O requests, nowhere does the cited col. 5 anywhere disclose determining whether a number of queued I/O requests exceeds a threshold. Instead, the cited col. 5 mentions that the queued requests are outputted as a burst.

The Examiner cited col. 6, lines 29-48 with respect to the pre-amended claim requirement of calculating a coalesce limit (Second Office Action, pg. 3). This limitation now requires that the calculation is in response to determining that the number of queued I/O requests exceeds the threshold. Applicants traverse with respect to the amended limitation.

The cited col. 6 mentions that queue control circuitry 204 conditions bursts of memory requests to crossbar 102 and memory 103 so the return queue 203 will not overflow. The queue control circuitry controls the burst size ($Burst_{max}$), which is a function of variables A and N, where N is the length of an output queue and A is the cycle at which elements are received and outputted from the output queue. Thus, with the cited col. 6 the burst size for a queue is calculated independent of the number of queued I/O requests. The claims require that the coalesce limit is calculated in response to determining that the number of queued I/O requests exceeds the threshold. Nowhere does the cited col. 6 anywhere disclose that the maximum burst size is calculated in response to determining that the number of queued I/O requests exceeds the threshold. Instead, the cited col. 6 mentions that the burst size is calculated as a function of A and N, which do not include the number of determined queued I/O requests.

Accordingly, claims 1 and 18 are patentable over the cited art because the cited Foster does not disclose all the claim requirements.

Claims 2, 3, 5, 6, 10, 19, 20, 22, 23, 27, and 28 are patentable over the cited art because they depend from one of claims 1 and 18, which are patentable over the cited art for the reasons discussed above. Moreover, the below discussed dependent claims provide further grounds of patentability over the cited art for the following reasons.

Claims 2 and 19 depend from claims 1 and 18 and further require that the calculated coalesce limit dynamically varies based in part on the number of queued I/O requests. The Examiner cited col. 6, lines 55-67 of Adkisson as disclosing the additional requirements of these claims. (Second Office Action, pg. 3) Applicants traverse.

The cited col. 6 mentions that the queue control circuitry controls the wait time between bursts from the queue 200 to ensure that two or more consecutive bursts occur sufficiently apart to allow queue 203 to empty between bursts of data words from memory 103.

Nowhere does the cited col. 6 anywhere disclose the claim requirement of dynamically varying a coalesce limit that indicates a number of I/O requests to coalesce to transmit. Instead, the cited col. 6 discusses when to burst or the wait time between bursts. Further, as discussed,

the previously cited col. 6 discusses that the burst size is a function of the length N of the output queue and cycle A at which elements received and outputted. Nowhere does the cited col. 6 anywhere disclose dynamically varying the coalesce limit or burst size in response to the determined number of queued I/O requests exceeding a threshold.

Accordingly, claims 2 and 19 provide additional grounds of patentability over the cited art because the cited art does not disclose the additional requirements of these claims.

Claims 3 and 20 depend from claims 2 and 19 and further require that calculating the coalesce limit includes dividing the number of queued I/O requests by an interval. The Examiner cited col. 6, lines 55-67 of Adkisson as disclosing the additional requirements of these claims. (Second Office Action, pg. 3) Applicants traverse.

The cited col. 6 mentions that the queue control circuitry controls the wait time between bursts from the queue 200 to ensure that two or more consecutive bursts occur sufficiently apart to allow queue 203 to empty.

Nowhere does the cited col. 6 anywhere disclose the claim requirement that the burst size or coalesce limit is calculated by dividing the number of queued I/O requests by an interval. Instead, the cited col. 6 discusses when to burst or the wait time between bursts. Further, as discussed, the previously cited col. 6 discusses that the burst size is a function of the length N of the output queue and cycle A at which elements received and outputted. Nowhere is there any disclosure or mention in the cited Adkisson that the burst size or coalesce limit is calculated by dividing the determined number of queued I/O requests by an interval.

Accordingly, claims 3 and 20 provide additional grounds of patentability over the cited art because the cited art does not disclose the additional requirements of these claims.

Claims 5 and 22 depend from claims 1 and 18 and further require that I/O requests are queued in a first queue or a second queue, wherein determining whether the number of queued I/O requests exceeds the threshold comprises determining whether a number of I/O requests in the second queue exceeds the threshold, and wherein coalescing the number of queued I/O requests comprises coalescing I/O requests from the first queue.

The Examiner cited the paragraph bridging columns 5 and 6 of Adkisson. (Second Office Action, pg. 4) The cited cols. 5 and 6 discuss two queues 200 and 201. During operation, memory requests are provided to memory unit 103 in bursts of 16. The queue 200 accumulates 11 requests before outputting them to queue 201 and queue 200 accumulates 5 more requests

from the I/O system 105 during this time to send a burst of 16. The burst length and frequency are programmable providing flexibility.

Although the cited col. 5 discusses how queue 200 bursts requests to queue 201, nowhere does the cited col. 5 anywhere disclose that a coalesce limit or burst size is calculated for one queue in response to determining that the number of queued I/O requests in another queue exceeds a limit. There is no mention in the cited col. 5 that the calculation of the burst size for one queue depends on the number of I/O requests in another queue.

Accordingly, claims 5 and 22 provide additional grounds of patentability over the cited art because the cited art does not disclose the additional requirements of these claims.

Claims 10 and 27 depend from claims 1 and 18 and additionally recite transmitting one I/O request from the queue if the number of queued I/O requests does not exceed the threshold. The Examiner cited col. 5, lines 35-45 of Adkisson as disclosing the additional requirements of these claims. (Second Office Action, pg. 4) Applicants traverse.

The cited col. 5 mentions that memory requests are received at an I/O queue. The requests to the queue 102 are outputted at a selected clock rate that is a multiple of the clock rate at which the memory units 103 inputs memory requests. When the memory clock rate exceeds the I/O output clock rate, queue 200 queues a number of memory requests, after which the queued requests are output to the memory unit 103 as a burst.

Although the cited col. 5 discusses a queue 200 bursting I/O requests, nowhere does the cited col. 5 anywhere disclose that one I/O request is transmitted if the number of queued I/O requests does not exceed a threshold. There is no disclosure in the cited Adkisson that the determination of a threshold with respect to queued I/O requests plays a role in determining whether to transmit one I/O request.

Accordingly, claims 10 and 27 provide additional grounds of patentability over the cited art because the cited art does not disclose the additional requirements of these claims.

2. Claims 4 and 21 are Patentable Over the Cited Art

The Examiner rejected claims 4 and 21 as obvious (35 U.S.C. §103) over Adkisson in view of Gunlock (U.S. Patent No. 5,522,054).

Applicants traverse because these claims depend on claims 1 and 18, which are patentable over the cited art for the reasons discussed above and because the additional

requirements of these claims in combination with the base claims provide further grounds of patentability over the cited art.

3. Claims 7, 8, 11-13, 15, 17, 24, and 25 are Patentable Over the Cited Art

The Examiner rejected claims 7, 8, 11-13, 15, 17, 24, and 25 as obvious (35 U.S.C. §103) over Adkisson in view of Marcotte (U.S. patent No. 6,292,856). Applicants traverse for the following reasons.

Claims 7, 8, 24, and 25 are patentable over the cited art because they depend from one of claims 1 and 18, which are patentable over the cited art for the reasons discussed above, and because the additional requirements of these claims in combination with the base claims provide further grounds of patentability over the cited art.

Claim 11 substantially includes the requirements of claims 1 and 18, with the additional requirement that the operations are performed by a device driver. The Examiner cited the sections of Adkisson cited above and cited Marcotte for the teaching of a device driver. Applicants submit that the cited Adkisson does not teach the requirements of claim 11 for which it is cited for the reasons discussed with respect to claims 1 and 18. Moreover, the cited Marcotte does not address the shortcomings of Adkisson.

Accordingly, claim 11 is patentable over the cited art for the reasons discussed with respect to claims 1 and 18.

Claims 12, 13, 15, and 17 are patentable over the cited art because they depend from claim 11, which is patentable over the cited art for the reasons discussed above. Moreover, claims 12, 13, 15, and 17 substantially include the requirements of claims 2, 3, 5, and 10. Thus, claims 12, 13, 15, and 17 provide additional grounds of patentability over the cited art for the reasons discussed above with respect to claims 2, 3, 5, and 10.

4. Claim 14 is Patentable Over the Cited Art

The Examiner rejected claim 4 as obvious (35 U.S.C. §103) over Adkisson in view of Marcotte and Gunlock.

Applicants traverse because claim 14 depends from claim 11, which is patentable over the cited art for the reasons discussed above and because the additional requirements of claim 14 in combination with the base claim provides further grounds of patentability over the cited art.

Conclusion

For all the above reasons, Applicant submits that the pending claims 1-28 are patentable over the art of record. Applicants have not added any claims. Nonetheless, should any additional fees be required, please charge Deposit Account No. 50-0585.

The attorney of record invites the Examiner to contact him at (310) 553-7977 if the Examiner believes such contact would advance the prosecution of the case.

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